AMENDMENTS TO THE CLAIMS

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) Error checking circuitry for performing error checks based on mathematical functions comprising:

a data input stage having a data node adapted to receive incoming data to be checked and a plurality of input feedback nodes;

a register having a plurality of data input nodes each data input node being selectable to receive data from the data input stage and a set of output feedback nodes arranged to selectively supply a feedback signal to the data input stage;

multiplexing circuitry provided in association with the register and the data input stage to selectively connect one of said output feedback nodes to the data input stage and to selectively connect said data node to at least some of the said data input nodes such that the signal routes through the error checking circuitry are configurable to successively perform error checks based on different mathematical functions;

wherein the register comprises a plurality of delay elements, each capable of holding one bit;

wherein the register further comprises a first data input node and a plurality of further data input nodes disposed between selected ones of the delay elements; and

wherein the multiplexing circuitry is arranged to selectively connect an incoming data signal from the input stage and a zero signal to said data input nodes of the register, and wherein said multiplexing circuitry comprises a multiplexor arranged to supply a common term signal to a plurality of said data input nodes..

2-4. (Canceled)

5. (Previously Presented) Error checking circuitry according to claim 1, wherein the multiplexing circuitry comprises combinatorial logic for combining the incoming data with a feedback signal from said register.

6. (Original) Error checking circuitry according to claim 5, wherein said multiplexing circuitry includes two combinatorial logic stages each comprising an XOR-gate.

7. (Original) Error checking circuitry according to claim 6, wherein the multiplexing circuitry includes two multiplexing stages each receiving an input from said combinatorial logic stages.

8. (Original) Error checking circuitry according to claim 7, wherein a multiplexor select signal indicating the mathematical function to be used is supplied to both said multiplexing stages.

9. (Previously Presented) Error checking circuitry according to claim 1, wherein the register comprises a number of delay elements sufficient to implement error checking based on a 32-bit CRC generator polynomial.

10. (Previously Presented) Error checking circuitry according to claim 1, wherein the incoming data comprises a digital video data stream.

11. (Previously Presented) Error checking circuitry according to claim 1, wherein certain ones of said further data input nodes are, in use employed in error checks based on both said 32-bit and 16-bit CRC generator polynomials.

12. (Currently Amended) A method of checking an incoming bit stream for errors, comprising the steps of:

receiving at an input stage an incoming bit stream;

supplying a plurality of input signals from said input stage to a register arranged to receive the plurality of input signals at a plurality of data input nodes, each data input node being selectable to receive said plurality of input signals, and to generate a plurality of feedback signals;

connecting one of said feedback signals to the input stage to perform an error check based on a first mathematical function;

subsequently disconnecting said feedback signal and connecting another one of said feedback signals to the input stage thereby to perform an error check based on a second, different, mathematical function; and

wherein said step of supplying said plurality of input signals is performed using the multiplexing circuitry is arranged to selectively connect an incoming data signal from the input stage and a zero signal to said data input nodes of the register, and wherein the multiplexing circuitry comprises a multiplexor arranged to supply a common term signal to a plurality of said data input nodes.

13-14. (Canceled)